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Sanjay Ghodawat University, Kolhapur

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2018-19
EXM/P/09/01

Year and Program:2018-19 Electrical & Electronics | **School of Technology** | **Department of Electrical & Electronics**
SY B.Tech
Course Code: EET 206 | **Course Title: Digital Electronics** | **Semester – II**

Day and Date Saturday 25-05-2019 | **End Semester Examination (ESE)** | **Time:** 3 Hrs. 10.30 am to 1.30 pm | **Max Marks: 100**

Instructions:
1) All questions are compulsory.
2) Assume suitable data wherever necessary.
3) Figures to the right indicate full marks.

		Marks	Bloom's Level	CO
Q.1	**Solve the following.**			
a)	List all characteristics of Digital ICs. Explain in Details any three.	07	L1	CO1
	OR			
a)	Compare CMOS & TTL Logic Family	07	L4	CO1
b)	State and prove associative, commutative, Distributive and Negation Laws of Boolean algebra.	08	L3	CO2
	OR			
b)	Write short notes on Demorgan's Theorem. Solve $\overline{(\bar{A}+B).(A+\bar{B})}$	08	L3	CO2
Q.2	**Solve the following.**			
a)	Differentiate between SOP and POS form. Write Minterm & Maxterm for 3 (A,B,C) variable.	07	L3	CO3
	OR			
a)	Reduce the expression F=$\sum m(0,2,3,4,5,6)$ using K-mapping & implement it in AOI Logic as well as in NAND Logic.	07	L4	CO3
b)	Explain Full Adder & implement it using 2 Half Adder.	08	L3	CO4
	OR			
b)	Design a 4-Bit Binary to Gray Code converter.	08	L4	CO4

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Q.3		**Solve any Two**			
	a)	Prove that 1. $A\bar{B}C+B+B\bar{D}+AB\bar{D}+\bar{A}C=B+C$ 2. $AB+\bar{A}C=(A+C)(\bar{A}+B)$	08	L3	CO1
	b)	Explain 2-Bit and 4-bit Magnitude comparator.	08	L3	CO2
	c)	Solve equation using Quine McCluskey method. $F(A,B,C,D)=\sum m(0,2,3,6,7,8,10,12,13)$	08	L3	CO3
	d)	Design the following logic function using 8:1 MUX $F(A,B,C,D)=\sum m(1,3,4,11,12,13,14,15)$.	08	L3	CO4
Q.4		**Solve any Two**			
	a)	Design and implement edge triggered D-flip flop.	09	L3	CO5
	b)	What is the shift register? Explain Parallel In Serial Out shift Register.	09	L3	CO5
	c)	Design 4-bit UP Ripple counter by using T-flip flops.	09	L3	CO5
Q.5		**Solve any Two**			
	a)	Explain Moore and Mealy machines in detail.	09	L3	CO5
	b)	Explain State Diagram, State Table, State Assignment and State Reduction Techniques.	09	L2	CO5
	c)	Explain in detail universal shift register.	09	L4	CO5
Q.6		**Solve any Three**			
	a)	Compare combinational and sequential Logic Circuits.	06	L3	CO5
	b)	Convert S-R flip-flop to J-K flip-flop.	06	L3	CO5
	c)	Design MOD-6 Asynchronous counter using T flip-flops.	06	L4	CO5
	d)	Explain about the twisted Ring counter (Johnson Counter).	06	L2	CO5

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